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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

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CERTIFICATE OF HAND DELIVERY

I hereby certify that this correspondence is being hand filed with the United States Patent and Trademark Office in Washington, D.C. on June 16, 2000.

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APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: **Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231**

1. [X] Fee Transmittal Form *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification [Total Pages 9] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC 113)* [Total Sheets 1]
4. [ ] Oath or Declaration [Total Pages]
   a. [ ] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 5 below]***
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
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ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement [ ] Power of Attorney *(when there is an assignee)*
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
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[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: _____

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dc-212954

☒ If a paper is untimely filed in the above-referenced application by applicant or his/her representative, the Assistant Commissioner is hereby petitioned under 37 C.F.R. § 1.136(a) for the minimum extension of time required to make said paper timely. In the event a petition for extension of time is made under the provisions of this paragraph, the Assistant Commissioner is hereby requested to charge any fee required under 37 C.F.R. § 1.17(a)-(d) to **Deposit Account No. 03-1952**. However, the Assistant Commissioner is **NOT** authorized to charge the cost of the issue fee to the Deposit Account.

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MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $260.00	$0.00
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Dated: June 16, 2000

Respectfully submitted,

By: _____

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SEMICONDUCTOR WAFER GRINDING METHOD

FIELD OF THE INVENTION

The present invention relates to a method for grinding a semiconductor wafer cut out from a semiconductor ingot.

BACKGROUND OF THE INVENTION

A semiconductor wafer used to fabricate a semiconductor device is generally manufactured through slicing, grinding, and polishing. That is, a semiconductor ingot that is a material of a semiconductor wafer is sliced by a wire saw or the like to form a thin discoid wafer. In this case, fluctuation occurs in thickness and flatness of a wafer depending on a slicing condition. Moreover, a machining-strain layer in a wafer may increase in size. Therefore, both sides of a wafer cut out from a semiconductor ingot are ground in order to uniform the thickness of the wafer, flatten the wafer, and remove machining-strain layers from the wafer and thereafter, the wafer passes though the polishing and is formed into a product (Japanese Patent Laid-Open Nos. 9-248758, 9-262746, 9-262747, 10-156681, 10-180599, and 10-277898).

The both side grinding of a wafer uses fixed abrasive grains or free abrasive grains. Grinding by fixed abrasive grains grinds a workpiece between so-called grindstones.

Grinding by free abrasive grains grinds a workpiece between rotating surface plates by supplying free abrasive grains between the plates, which is referred to as lapping. It is said that the efficiency of grinding by fixed abrasive grains using a grindstone is exceptionally higher than that of grinding by free abrasive grains.

Grinding by fixed abrasive grains using a grindstone and lapping by free abrasive grains use large diameter abrasive grains because a sliced wafer (wafer to be ground) has a rough

surface. In case of grinding by fixed abrasive grains, a holding force for the grindstone tends to increase as the diameter of an abrasive grain increases. Then a surface to be ground is rough, abrasive grains are extremely removed from a grindstone unless the grains have a large diameter and thereby, machining becomes impossible in a short time.

SUMMARY OF THE INVENTION

When large diameter abrasive grains are used to grind both sides of a semiconductor wafer, not only is a sufficient surface roughness not obtained, but also a machining-strain layer is formed in a range of approx. 10μ m from the surface of the wafer due to the grinding itself. Therefore, it is necessary to finish grind both sides of the wafer by using small diameter abrasive grains before starting grinding in the next step and thereby, the efficiency is inevitably lowered.

To perform finish grinding by fixed abrasive grains, fine fixed abrasive grains are necessary. In case of grinding by fixed abrasive grains, abrasive grains are more violently removed as the grain diameter decreases and thereby, stable machining is difficult. Therefore, a problem occurs that machining becomes unstable.

In case of grinding by fixed abrasive grains, it cannot be avoided that grinding marks are left even if finishing is performed by small diameter abrasive grains. In case of a one-side polishing wafer, an error occurs when chucking the wafer through vacuum attraction if grinding marks are left on the back of a wafer. Therefore, both side grinding by fixed abrasive grains cannot be applied to a one-side polishing wafer. Because a one-side polishing wafer must depend on low efficiency lapping, the efficiency is further lowered.

It is an object of the present invention to provide a semiconductor wafer grinding method capable of efficiently supplying a high quality grinded wafer to polishing in the next step. A

semiconductor wafer grinding method consistent with the present invention grinds a semiconductor wafer by fixed abrasive grains and then, continuously grinds the wafer by free abrasive grains on the same grinding axis.

Grinding by free abrasive grains on the same grinding axis is performed by supplying free abrasive grains to a grinding portion in the form of grinding by fixed abrasive grains. That is, grinding by free abrasive grains on the same grinding axis uses a grindstone for grinding by fixed abrasive grains as a surface plate for grinding by free abrasive grains.

To perform grinding by free abrasive grains, it is preferable to lower the grinding action by fixed abrasive grains in order to completely reveal the grinding action. As a specific method for lowering the grinding action by fixed abrasive grains, the following is considered: lowering of a feed rate of a grindstone or a combination between lowering of a feed rate of a grindstone and lowering of a rotational speed. It is preferable to set a feed rate and a rotational speed of a grindstone for grinding by free abrasive grains to 10 to 15% of a feed rate and 5 to 10% of a rotational speed of a grindstone for grinding by fixed abrasive grains. In this connection, it is preferable to set a grindstone feed rate for grinding by fixed abrasive grains to 0.1 to 0.2 mm/min and a grindstone rotational speed to 2,500 to 3,000 rpm.

Using such operations, in a semiconductor wafer grinding method of the present invention, finish grinding is continuously and efficiently performed after rough grinding by fixed abrasive grains without changing grindstones on the same grinding axis.

That is, by rough grinding using large diameter fixed abrasive grains in the first half of grinding, it is possible to machine a sliced semiconductor wafer having a rough surface in a comparatively short time. Moreover, it is possible to flatten the sliced wafer and set the flatness to 1 to 2 μ m in TTV (Total Thickness Variation). Furthermore, by securing a sufficient

machining margin through the rough grinding, it is possible to control a machining-strain layer produced through the rough grinding itself to approx. 10 μ m from the surface of the wafer while removing the machining-strain layer produced through slicing.

Moreover, by continuously performing finish grinding itself using small diameter free abrasive grains on the same grinding axis after the rough grinding, it is possible to control a machining-strain layer produced through the finish grinding itself to 2 to 3 μ m from the surface of the wafer while removing the machining-strain layer produced through the rough grinding, and also to make TTV (Total Thickness Variation) μ m or less.

Thus, in case of a semiconductor wafer grinding method of the present invention, a high accuracy grinding wafer is efficiently obtained in one efficient step mainly including grinding using fixed abrasive grains. Moreover, because finish grinding is grinding by free abrasive grains, it is possible to form a satin finished surface necessary for a one-side polishing semiconductor wafer.

It is preferable to set a machining margin in the first half of grinding by fixed abrasive grains so as to be able to completely flatten a sliced wafer and remove a machiningstrain layer produced through slicing. Specifically, it is preferable to set the margin to 50 to 60 μ m. Moreover, it is preferable to set a machining margin in the latter half of grinding by free abrasive grains so as to be able to remove the machining-strain layer produced in the first half of grinding. Specifically, it is preferable to set the margin to 10 to 20 μ m.

A grain size of #325 to #1000 is preferable for fixed abrasive grains. When a diameter of the fixed abrasive grain is too small, the efficiency lowers and when the diameter is too large, a machining-strain layer produced through the grinding concerned becomes thick and thereby the efficiency extremely lowers in the latter half of the grinding by free abrasive grains. A grain size

of #2000 to #8000 is preferable for free abrasive grains. The efficiency lowers when a diameter of the free abrasive grain is too small and a machining-strain layer produced through the grinding concerned becomes thick when the diameter is too large.

A semiconductor wafer grinding method of the present invention can be applied not only to both side grinding of a semiconductor wafer but also to grinding of a chamfered portion.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a grinder suited to execute a semiconductor wafer grinding method of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

An embodiment of the present invention will be described below by referring to the accompanying drawing. FIG. 1 is a block diagram of a grinder suitable to execute a semiconductor wafer grinding method of the present invention.

The grinder shown in FIG. 1 is provided with a pair of top and bottom grindstones I and 2 arranged on the same line. The grindstones 1 and 2 serving as fixed grindstones rotate in the same direction or opposite directions at a high speed and are feed in the axial direction. A semiconductor wafer 3 serving as a workpiece is held between the grindstones 1 and 2 at a position eccentric to the rotation center of the grindstones 1 and 2 and rotates at a low speed. Thereby, both sides of the semiconductor wafer 3 are roughly ground by fixed abrasive grains.

The upper stage grindstone 1 is equipped with slurry pipes 4 and 4. The slurry pipes 4 and 4 rotate together with the grindstone 1 to supply a slurry which suspends fine abrasive grain, serving as free abrasive grains between the grindstones 1 and 2. The lower stage grindstone 2 is also equipped with slurry pipes 5 and 5. The slurry pipes 5 and 5 rotate together with the

grindstone 2 to supply a slurry which suspends fine abrasive grain, serving as free abrasive grains between the grindstones 1 and 2. Thereby, both sides of the semiconductor wafer 3 are simultaneously finish ground by free abrasive grains between the grindstones 1 and 2.

To execute a semiconductor wafer grinding method of the present invention, both sides of the semiconductor wafer 3 are rough ground by rotating the semiconductor wafer 3 between the grindstones 1 and 2 at a low speed while driving the grindstones 1 and 2 at predetermined rotational speed and feed rate. After continuing rough grinding for a predetermined time, both sides of the semiconductor wafer 3 are continuously finish ground on the same grinding axis by continuing rotation of the grindstones 1 and 2 and the semiconductor wafer 3 while supplying a slurry which suspends fine abrasive grain between the grindstones 1 and 2 from the slurry pipes 4 and 4 and 5 and 5.

For finish grinding, the rotational speed and feed rate of the grindstones 1 and 2 are lowered compared to the case of rough grinding.

Thereby, both sides of the semiconductor wafer 3 are efficiently ground up to a necessary high accuracy before polishing without changing grindstones or using a lapping machine together.

Both sides of a silicon wafer having a diameter of 200 mm were actually ground in accordance with the above method.

That is, rough grinding was performed for 90 sec by setting a number of the abrasive grain for the grindstones 1 and 2 to #600, a rotational speed of the grindstones 1 and 2 to 2, 500 rpm, a feed rate of the grindstones 1 and 2 to 0. 3 mm/min, a rotational speed of the semiconductor wafer 3 to 10 rpm and thereafter, finish grinding was performed for 60 sec by setting free abrasive grain used for fine abrasive grain slurry to #2, 500, a slurry flow rate to

0.01 m^3 /min, a rotational speed of the grindstones 1 and 2 to 200 rpm, a feed rate of the grindstones 1 and 2 to 0.02 mm/min, and a rotational speed of the semiconductor wafer to 3 to 10 rpm.

The ground semiconductor wafer was taken out of the grinder to examine the surface roughness and TTV (Total Thickness Variation) of the wafer. Table 1 shows the examination results.

As shown in Table 1, though the surface roughness was 18 μ m after slicing, it was improved up to 1 μ m. Though TTV (Total Thickness Variation) was 20 μ m after slicing, it was improved up to 0.5 μ m. The total duration was 2 min 30 sec (90 sec + 60 sec).

In this connection, the surface roughness levels off at 3 μ m and TTV (Total Thickness Variation) levels off at 1.5 μ m only through rough grinding by fixed abrasive grains. To perform finish grinding by free abrasive grains with another equipment after rough grinding by fixed abrasive grains, two types of equipments are necessary and moreover, wafer transfer between equipments is necessary.

Moreover, the total duration when performing all steps from rough grinding up to finish grinding only by free abrasive grains reaches approx. 22 min.

Table 1

	Slicing	Rough grinding (Fixed abrasive grain)	Finish grinding (Free abrasive grain)
Surface roughness (Rmax, μm)	18	3	1
TTV (μm)	20	1.5	0.5

As described above, a semiconductor wafer grinding method of the present invention makes it possible to efficiently supply a high accuracy grinding wafer to the next polishing step by performing grinding by fixed abrasive grains and then performing grinding by free abrasive grains in the same grinding axis. Therefore, it is possible to reduce the wafer production cost, efficiently supply a high accuracy grinded wafer to the next polishing step, and also reduce the production cost.

What is claimed is:

1. A semiconductor wafer grinding method, comprising:

grinding a semiconductor wafer by fixed abrasive grains; and

continuously grinding the semiconductor wafer by free abrasive grains.

2. The semiconductor wafer grinding method according to claim 1, wherein:

grinding by fixed abrasive grains includes rough grinding using large diameter abrasive grains; and

grinding by free abrasive grains includes finish grinding using small diameter abrasive grains.

3. The semiconductor wafer grinding method according to claim 1, wherein grinding includes both side grinding of a semiconductor wafer or grinding of a chamfered portion.

FIG 1